

# PPF5200AMMGAES – NXP Standard

## Configuration report for PF5200-QM OTP program ID: GA rev A

Rev. 1.0 - 5/18/2022

Report

### 1 General description

The PF5200 integrates multiple high performance buck regulators. It can operate as a stand-alone point-of-load regulator IC, or as a companion chip to a larger PMIC.

Built-in one-time programmable (OTP) memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states.

### 2 Features and benefits

- Two high efficiency buck converters
- Watchdog timer/monitor
- Monitoring circuit to fit ASIL B safety level
- One-time programmable device configuration
- 3.4 MHz I2C communication interface
- 32-pin FC-QFN package with wettable flank

### 3 Applications

- Automotive Infotainment
- High-end consumer and industrial

### 4 Ordering information

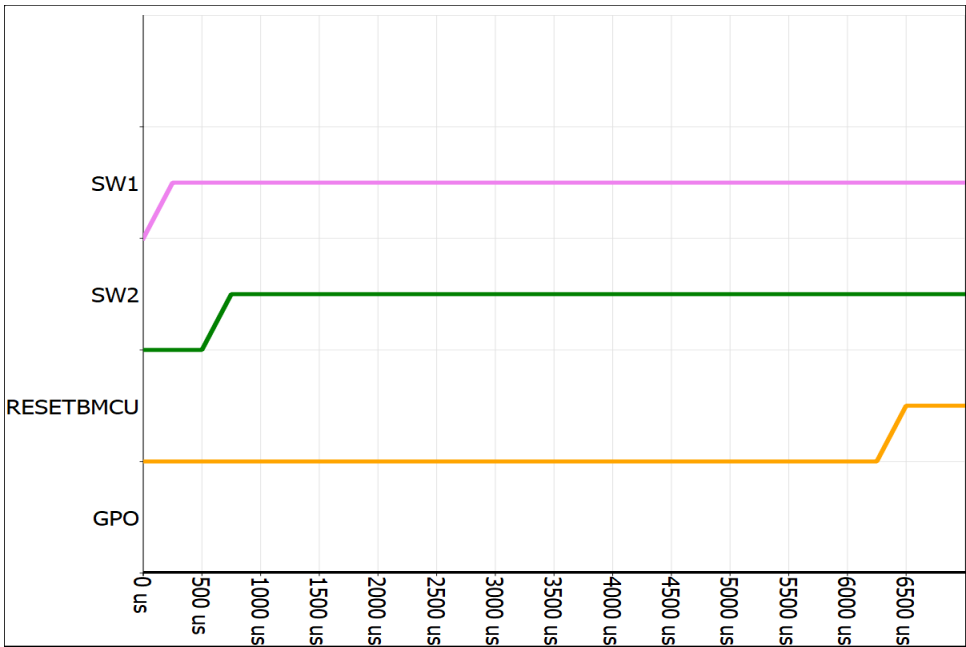
Table 1. Ordering information

Type number <sup>[1]</sup>	Package		
	Name	Description	Version
PPF5200AMMGAES	HWQFN32	Plastic thermal enhanced very thin quad flat pack; no leads, wettable flank, 32 terminals, 0.5 mm pitch, 5 mm x 5 mm x 0.68 mm body	SOT2039 - 2(SC)

[1] To order parts in tape and reel, add the R2 suffix to the part number.

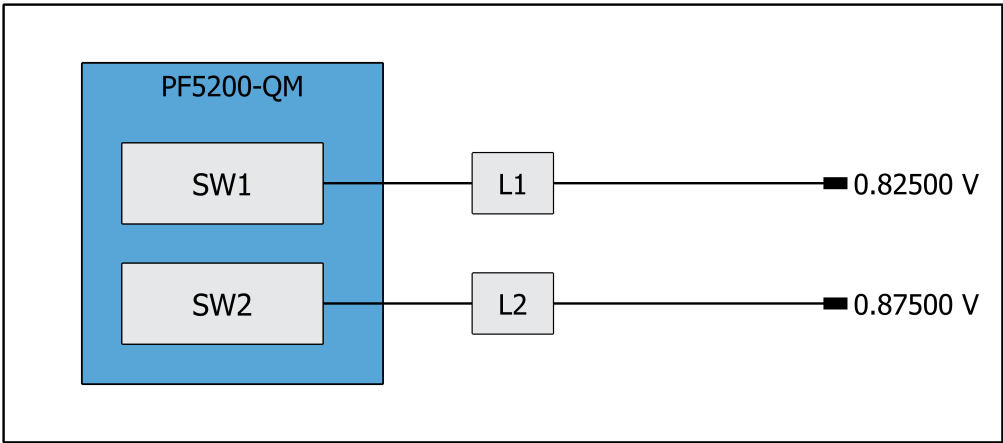


5 Power-up sequence summary



The signals depicted above are enable signals for each regulator. They don't represent the actual ramp voltage.

6 Hardware configuration diagram



## 7 OTP configuration

See PF5200 datasheet for parametric details. The OTP configuration summary for GA sequence ID is provided in Tables below.

**Table 2. Device OTP configuration**

Functional block	Feature	OTP selection
System Configuration	I2C Address	0x09
	I2C CRC	Disabled
	VIN_OVLO Mode	Enabled
	VIN_OVLO Shutdown	Interruption only on VIN_OVLO
	Maximum Fault Counter	Disabled
	Fault Timer	Disabled
I/O CONFIGURATION	Power On Event Detection	Level sensitive
	PWRON Debounce	Falling Edge - 32 ms and Rising Edge - 32 ms
	TRESET Behavior	Shutdown
	TRESET Time	2 s
	PGOOD Pin Operation	PGOOD Mode
	PG Check On Power Up	PG not checked at power up
	EWARN Delay	5 ms
	XFAIL Operation	Enabled
Watchdog Monitoring	WD Timer	Disabled
	WD Window Duration	1024 ms
	WD Clear Window	Cleared within 100 % timer
	WD Expire Number	Event on step 7
	Maximum WD Event Counter	15 Events

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Clock Management	Nominal Switching Frequency	2.250 MHz
	SYNC Mode	Disabled
	SYNCIN Range	2000 KHz to 2500 KHz
	SYNCOUT Enable	Disabled
	Frequency Spread Spectrum	Enabled
	FSS Range	+/-5 %

Table 3. Power Sequencer configuration

Functional block	Feature	OTP selection
Power Up Sequence	Sequence Time Base	250 us
	SW1 Sequence Slot	Slot 0
	SW2 Sequence Slot	Slot 2
	RESETBMCU Sequence Slot	Slot 25
	PGOOD Sequence Slot	OFF
Power Down Sequence	Power Down Mode	Sequential
	SW1 Power Down Group	Group 4
	SW2 Power Down Group	Group 4
	RESETBMCU Power Down	Group 4
	PGOOD Power Down Group	Group 4
	Power Down Delay	10 ms
Power Down Delay	Group 1 Power Down Delay	120 us
	Group 2 Power Down Delay	120 us
	Group 3 Power Down Delay	120 us
	Group 4 Power Down Delay	120 us
	RESETBMCU Group Delay	No delay

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Table 4. SW Regulator configuration

Functional block	Feature	OTP selection
SW1	Output Voltage	0.82500 V
	UV Detection Threshold	95 %
	OV Detection Threshold	105 %
	Current Limit	11.0 A
	Output Inductor	0.47 uH
	Switching Phase	45°
	PGOOD Mode	Enabled
	SW1 OV Bypass	Protective behavior enabled
	SW1 UV Bypass	Protective behavior enabled
	SW1 ILIM Bypass	Interrupt only enabled
	DVS Ramp	7.03/4.69 mV/us
	SW1 Gain Margin	65 GM
SW2	Output Voltage	0.87500 V
	UV Detection Threshold	95 %
	OV Detection Threshold	105 %
	Current Limit	11.0 A
	Output Inductor	0.47 uH
	Switching Phase	90°
	PGOOD Mode	Enabled
	SW2 OV Bypass	Protective behavior enabled
	SW2 UV Bypass	Protective behavior enabled
	SW2 ILIM Bypass	Interrupt only enabled
	DVS Ramp	7.03/4.69 mV/us

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	SW2 Gain Margin	65 GM
SW Miscellaneous	Switching Mode	PWM
	SW1 Multi-phase Selector	SW1 and SW2 single phase

Table 5. PROGRAM ID

Functional block	Feature	OTP selection
PROGRAM ID	Program ID High	G
	Program ID Low	A

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